A Zero Inductor-Voltage 48V to 12V/70A Converter for Data Centers with 99.1% Peak Efficiency and 2.5kW/in^3 Power Density

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***Abstract*—The demand for internet and computing resources has led to datacenters and servers being one of the fastest growing consumers of power in the world today. While datacenter power architectures have improved over time, the majority of the loss still occurs at the server power supply, and board level voltage regulators. To attempt to improve this, Google has proposed and implemented a 48 volt server architecture that can significantly reduce both the upstream conversion losses, and the distribution losses within the server racks. Google has estimated that this change can reduce their overall conversion losses by up to 30%, but to fully realize these benefits new technology is needed to convert 48 volts down to the point of load voltage levels. The Intermediate Bus Architecture, where a "bus converter" steps down the 48 volts to a lower bus voltage which is then stepped down by point-of-load regulators is a very attractive option to "bridge the gap" between the 48 volt architecture of cutting edge servers, and the existing 12 volt architecture. The proposed topology is a novel intermediate bus converter that can achieve up to 2500W/in^3 power density, 99.1% peak efficiency, and 97.2% full load efficiency for 70A 12V output. Compared with other cutting edge designs this work achieves higher efficiency, and superior power density without the need for complex control, or a sensitive resonant based design.**

Keywords—DC-DC Converter, Datacenter, Intermediate Bus

I. Introduction

Switched Capacitor (SC) converters have seen a resurgence of research interest in recent years particularly for 48V to 12V conversion in next-generation data center applications. SC converters offer the advantage of reduces reliance on magnetic components compared to PWM-based converters, however, the problems associated with the charge redistribution loss results [3] in needing to use very large flying capacitor values, and higher switching frequencies, reducing power density and efficiency. In order to circumvent the problem associated with the charge redistribution loss SC topologies that incorporate an added inductive element have been proposed. According to [12], however, there are several key factors preventing the adoption of these topologies in industry. Firstly, for mass production the converter topologies must be highly immune to component non-idealities, such as component tolerance. Secondly, the MOSFETs ideally should be driven with a symmetrical, 50% duty cycle to minimize the RMS currents through the circuit components. Finally, scalability to higher power levels is extremely important as in conduction-loss dominated converters utilizing multiple phases can result in significant efficiency and power density improvements. While many SC topologies with added inductors cannot satisfy these criteria, the 12-Switch ZIV converter [1] has been demonstrated to satisfy the first two criteria, with all MOSFETs being driven at 50% duty cycle, and the PWM-based non-resonant design guaranteeing immunity to component non-idealities. In order to demonstrate the scalability to higher power levels, a Two-Phase 12-Switch ZIV converter is presented in this work. Additionally, with a Two-Phase 12-Switch ZIV converter operating at interleaving mode the input capacitor size and ESR loss are significantly reduced, which is particularly valuable as the input capacitor has the highest voltage stress, and therefore is the largest size component, in a one-phase 12-Switch ZIV converter. As shown in Figure 1 non-isolated unregulated topologies can offer huge gains in terms of both power density, and efficiency. Notably, the cascaded resonant converter presented in [17] achieves a power density of 2.2kW/in^3 and a full load, 12V/40A output efficiency of 97.8%. A further improved design based on the same topology [18] achieved 12V/60A output with an efficiency of 97.2% and a power density of 2.5kW/in^3. The Two-Phase 12-Switch ZIV converter presented in this paper achieves a power density of 2.5kW/in^3, including all input and output capacitors, matching the highest previously demonstrated in literature, along with a full load 12V/70A efficiency of 97.2%, and a 12V/60A efficiency of 97.8%, this achieving the highest efficiency for this high current level yet demonstrated for 48V to 12V conversion.

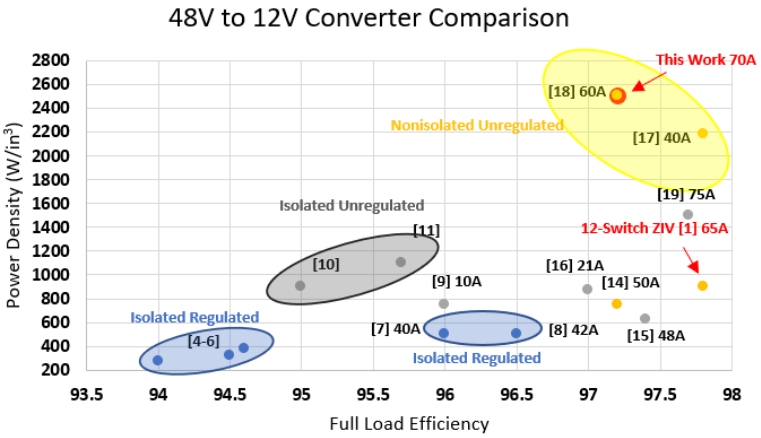

Figure 1 Comparison of Converter Topologies for 48V to 12V Conversion Referenced From [2]

II. Topology Overview

The 12-Switch ZIV converter is an unregulated, nonisolated stepdown converter topology. Utilizing a multilevel structure to reduce the voltage stress of the converter components, as well as the unique "zero inductor-voltage property" where the output inductor sees only the flying capacitor ripple, the ZIV converter is able to achieve power density and efficiency that exceed the highest previously demonstrated for 48V to 12V conversion

A. Operating Principles

The Two-Phase 12-Switch ZIV Converter topology is shown in Figure 2, along with the gate drive waveforms for one phase shown in Figure 3.

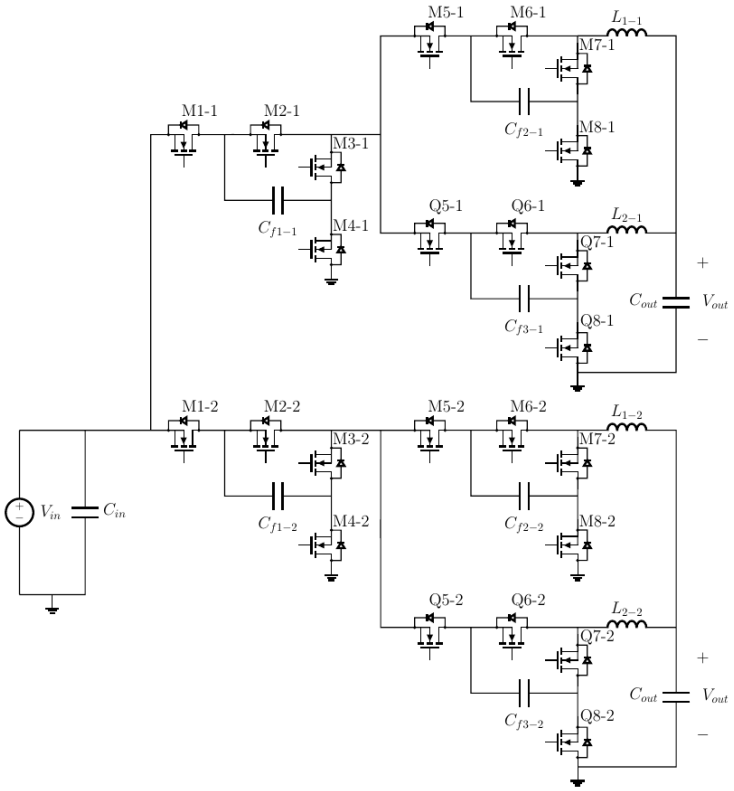

Figure 2 Two-Phase 12-Switch ZIV Converter Topology

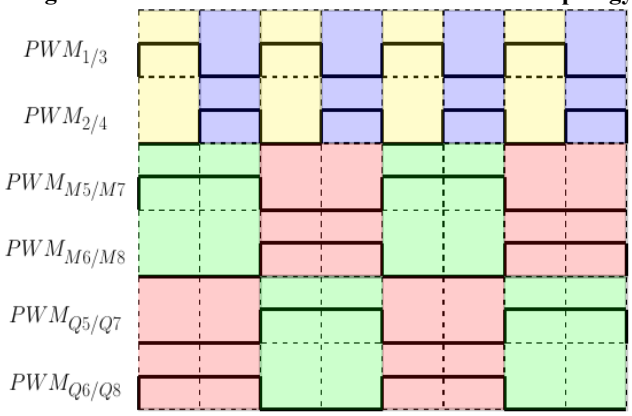

Figure 3 12-Switch ZIV Converter PWM Gate Diagram

The work presented in this paper utilizes a Two-Phase 12-Switch ZIV converter with interleaving operation. Both phases thus share an input capacitor connection, and operate with 180-degree phase shift. The key advantages of this topology over many SC topologies is that the flying capacitors are never connected in parallel, completely avoiding the charge redistribution loss, and, as compared with PWM based converters, the ZIV topology can operate at low frequency with a very small output inductor (200nH in this work) as the inductor sees only the capacitor ripple voltage. This low frequency operation substantially reduces the converter switching losses, without relying on a sensitive resonant based design. The modelled loss breakdown for the Two-Phase 12-Switch ZIV converter operating at 70A load, with parameters matching Table 1, is presented in Figure 4. Notably, over 85% of the total converter loss is conduction loss. This means that the ZIV converter can be referred to as a "conduction-loss dominated converter". A conduction loss dominated converter is particularly attractive for high current applications as utilizing multiple phases can them dramatically improve performance in terms of both size and efficiency.

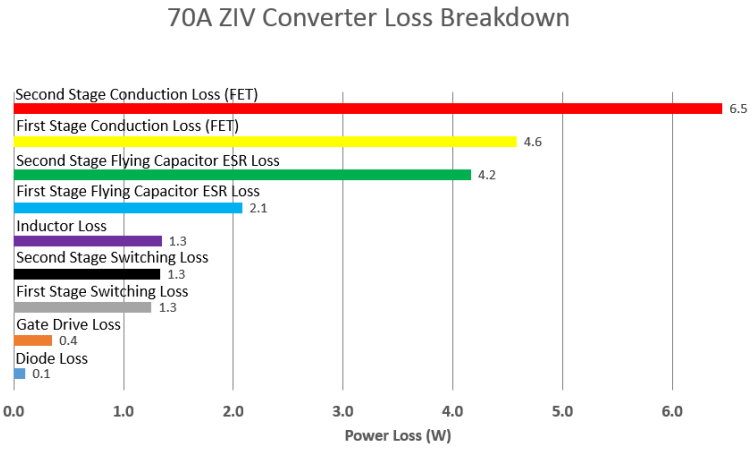

Figure 4 Two-Phase 12-Switch ZIV Converter Loss Breakdown

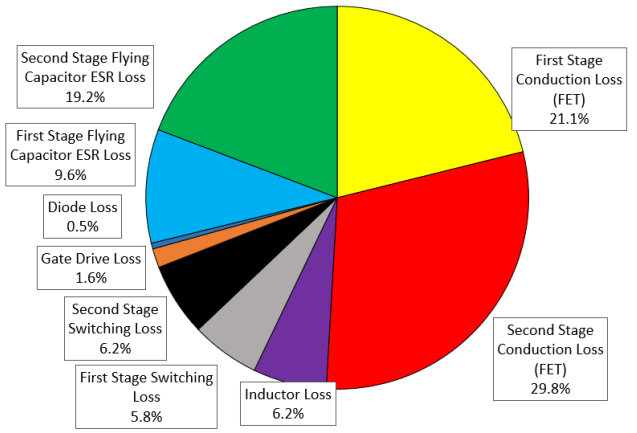

Figure 5 Two-Phase 12-Switch ZIV Converter Loss Breakdown

III. Comparison With Existing Topologies

A. Cascaded Resonant Converter

As shown in Figure 1 the Cascaded Resonant Converter demonstrates the highest efficiency and power density for a 48V to 12V converter outside of the ZIV converter family. One phase of a cascaded resonant converter is shown in Figure 6, referenced from [18].

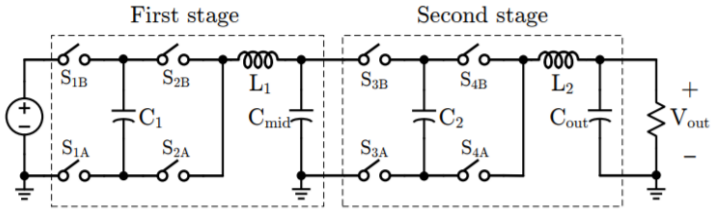

Figure 6 Cascaded Resonant Converter Referenced From [18]

As compared with the 12-Switch ZIV converter, the cascaded resonant converter requires 4 fewer MOSFETs (and associated driver circuitry). However, the cascaded resonant converter requires the middle network of L_1 and C_{mid} Additionally, as there is only one output stage, the output inductor L_2 will see substantially higher current for one phase of a cascaded resonant converter than a 12-Switch ZIV converter producing equal output current. Overall, this means that while the cascaded resonant converter is able to utilize fewer semiconductor devices, this is more than offset by the additional passive components required in the cascaded resonant converter.

Unlike the ZIV converter, the cascaded resonant converter achieves ZCS operation. This reduces the switching loss of the cascaded resonant converter. However, the output capacitor RMS current will be increased proportionally to the output inductor ripple current. This means that while ZCS operation reduces the switching loss, it does introduce some additional conduction loss in the output capacitor that offset this benefit. The ZCS operation of the cascaded resonant converter also does not perfectly eliminate the switching losses of the MOSFETs. ZVS operation is possible, as demonstrated in [18], allowing for better light load performance to be achieved. However, the ZVS technique proposed negatively impacts the converter performance at full load as compared with the ZCS operation of the cascaded resonant converter.

As noted in Figure 4 the ZIV converter is a conduction loss dominated converter. This means that although the ZIV converter does not use resonant operation to achieve ZCS or ZVS, the switching losses are minimized through several advantages of the topology. The MOSFET switching loss is proportional to the switching frequency, the current at the time of switching, the MOSFET voltage stress, and the turn-on/turn-off time of the MOSFET. In the ZIV converter, the switching frequency is extremely low (60kHz in this work). This is because the output inductor sees only the flying capacitor ripple voltage, thus allowing for low frequency operation. The multilevel structure of the ZIV converter allows for lower voltage stress MOSFETs to be utilized (40V MOSFETs for M1-M4, 25V MOSFETs for M5-M8 and Q5-Q8). This not only reduces the MOSFET voltage stress at the time of switching, but also allows for devices with substantially faster turn-on and turn-off times to be used as the figure-of-merit (FOM) for a MOSFET depends on its maximum voltage rating. Finally, while the ZIV converter does not achieve full ZCS operation, the output inductor current ripple does reduce the instantaneous MOSFET current during certain switching transitions. As the current is shared between two output stages, the second stage MOSFETs carry relatively low current during switching operation. All these factors combined allow the ZIV converters to achieve very low switching losses without relying on resonant operation.

In the 12-Switch ZIV converter, two output stages are used. These output stages share the output current, significantly reducing the conduction loss of the converter. For example, for 35A total output current each output stage would only deliver 17.5A of current. In the cascaded resonant converter the single output stage would deliver the full 35A of output current. This means that while the 12-Switch ZIV converter utilizes more semiconductor devices, the overall conduction loss is lower, and the cascaded resonant converter utilizes more passive components. Overall this means the ZIV converter is able to achieve higher efficiency, and power density, without the need for a resonant design.

B. ZIV Converter Family

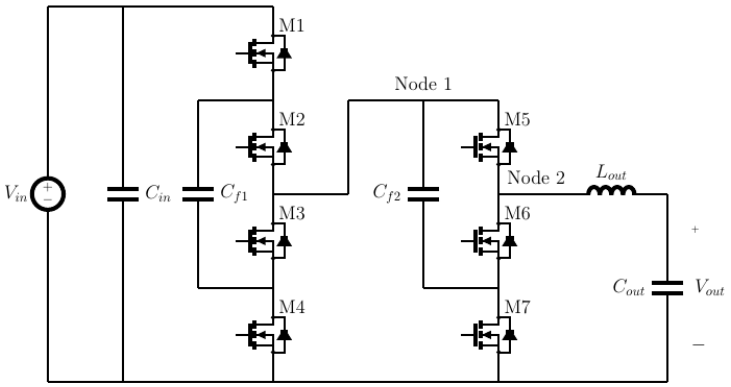

Figure 7 7-Switch ZIV Converter Topology

There are two primary topologies that make up the ZIV converter family. The first is the 7-Switch ZIV converter topology, shown in Figure 7, first introduced in [20]. The second is the 12-Switch ZIV converter topology, which this work is based on. The primary disadvantage of the 7-Switch ZIV converter topology is that the first stage MOSFETs, M1-M4, operate with only a 25% duty cycle. As outlined in [12] it is optimal to operate all switches with 50% duty cycle to achieve optimal utilization of the semiconductor devices. This is exemplified by the 12-Switch ZIV converter topology, which achieves 50% duty cycle on all MOSFET pairs by increasing the switching frequency of the input stage to twice that of the output stages.

As compared with a Two-Phase 7-Switch ZIV converter constructed of two 7-Switch ZIV converters operating in parallel, the 12-Switch ZIV converter utilizes two fewer MOSFETs and, more significantly, eliminates one flying capacitor. As detailed in [1] the 12-Switch ZIV converter, compared with a Two-Phase 7-Switch ZIV converter, achieves

very similar overall efficiency, with the only efficiency penalty coming from the addition of MOSFETs Q5 and M5. Figure 8 shows the approximate current waveforms for one "phase" of the 12-Switch ZIV converter consisting of M1-M8.

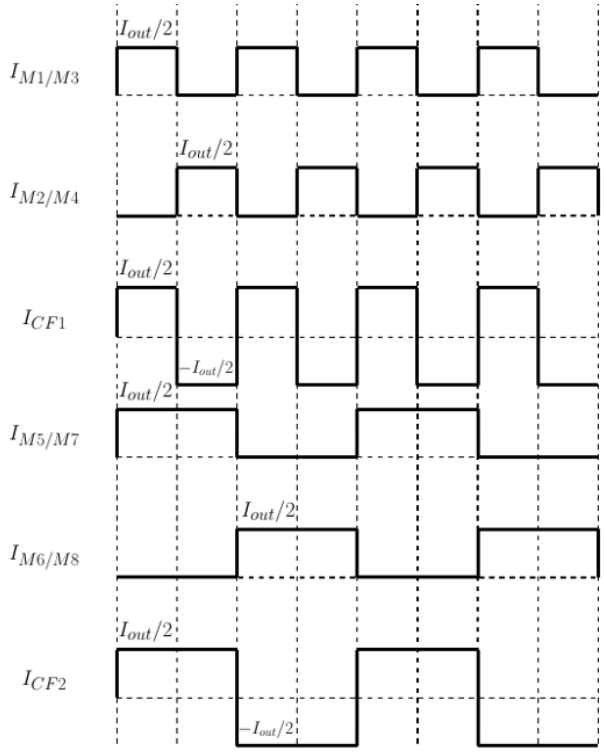

Figure 8 12-Switch ZIV Converter Approximate Current Waveforms

These waveforms can be used to demonstrate how the 12-Switch ZIV converter offers similar overall efficiency with a Two-Phase 7-Switch ZIV converter despite the significant component count reduction. First, while the switching frequency of the first stage (M1-M4) is doubled, the number of devices is halved, keeping the overall switching loss for the first stage the same. For the second stages, the addition of two high-side MOSFETs (M5 and Q5) is the only change that impacts efficiency when compared with the Two-Phase 7-Switch ZIV converter. Therefore, the total switching related loss is not increased by the higher frequency of the input stage, but only due to the addition of the two MOSFETs in the second stage. In the ZIV converter, however, the conduction loss is the dominant source of loss [8]. In a Two-Phase ZIV converter the input stage MOSFET current stress for each of the 8 MOFETs is given by:

$$I_{RMS} = \sqrt{0.25}\frac{I_{out}}{2} \text{ (each FET)} \quad (1)$$

For the 12-Switch ZIV converter the MOSFET current stress for each of the 4 input MOSFETs is:

$$I_{RMS} = \sqrt{0.5}\frac{I_{out}}{2} \text{ (each FET)} \quad (2)$$

The total conduction loss for the Two-Phase 7 -Switch ZIV converter input stage is then:

$$P_{cond} = 8\frac{I_{out}^2}{16}R_{ds(on)} = \frac{I_{out}^2}{2}R_{ds(on)} \quad (3)$$

For the 12-Switch ZIV converter:

$$P_{cond} = 4\frac{I_{out}^2}{8}R_{ds(on)} = \frac{I_{out}^2}{2}R_{ds(on)} \quad (4)$$

Noting that the Two-Phase ZIV converter has 8 devices compared with only 4 for the 12-Switch ZIV converter it is then clear that the overall conduction loss for the input stage is equal for both topologies. As the flying capacitors carry the same currents as the MOSFETs, the overall conduction loss of the flying capacitors is also the same between both converter topologies. It is then clear that the overall loss between both converters is nearly identical, with the addition of M5 and Q5 being the only additional sources of loss.

Due to the significant power density advantage offered by the 12-Switch ZIV converter, coupled with the minimal efficiency penalty, this makes the 12-Switch ZIV converter the superior option for applications, such as datacenter power supplies, where achieving high power density is critical.

IV. Analysis and Design

A. Current Sharing

One of the challenges associated with multiphase converters is ensuring adequate current sharing performance between the phases. In the case of the ZIV converter, the current sharing can be achieved passively through the output voltage "droop" characteristic of the ZIV converter. In an ideal converter, the ZIV converter will achieve exactly 4:1 stepdown. In the practical case, however, the output voltage will always be slightly lower than the expected value of Vin/4. This is because of the voltage drop associated with conduction through the components of the converter, including the MOSFETs, capacitors, PCB traces, and inductors. This gives the practical ZIV converter an output voltage characteristic that decreases linearly with output current. A theoretical, modelled output voltage characteristic for a ZIV converter is presented in Figure 9.

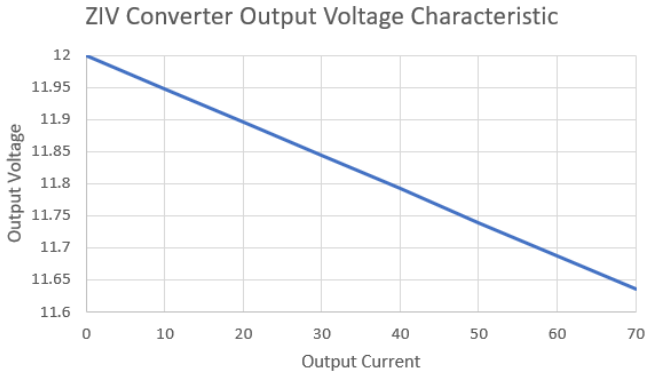

Figure 9 Modelled Two-Phase ZIV Converter Output Voltage

This negative output voltage characteristic allows for current sharing to be achieved passively by the ZIV converter family. The key principal is that the multiple phases of the ZIV converter are all essentially connected in parallel, with the same output voltage node. This means that all phases must output the same voltage.

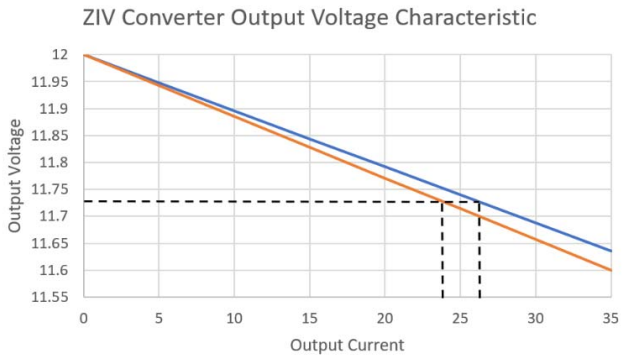

Figure 10 Two-Phase ZIV Converter with 10% Resistance Mismatch

Considering the case where two ZIV converters are paralleled with differing output voltage characteristics, the current will be shared according to this output voltage characteristic of each individual phase. If R_{ph1} and R_{ph2} are the lump equivalent resistance for each phase of the ZIV converter then the current sharing is given by:

$$I_{ph1} = I_{out}\frac{R_{ph2}}{R_{ph1}+R_{ph2}} \quad (5)$$

$$I_{ph2} = I_{out}\frac{R_{ph1}}{R_{ph1}+R_{ph2}} \quad (6)$$

Figure 10 demonstrates a case where there is a 10% mismatch in the output voltage characteristic of each converter, due to a 10% increase in the component resistances of one phase. For a 50A total load with 10% resistance increase in one phase relative to the other, the output voltage will be approximate 11.73V for 48V input. The current will share according to the equations:

$$I_{ph1} = 26.2A \quad (7)$$

$$I_{ph2} = 23.8A \quad (8)$$

For this modelled output characteristic, with an output voltage of 11.73V, the first phase will carry approximately 26.2A, while the second phase will carry approximately 23.8A. This negative output voltage characteristic does not guarantee perfect current sharing in the practical converter, due the potential for component tolerance mismatches, however, it does guarantee that reasonably good current sharing can be achieved passively with no additional control required.

Additionally, MOSFETs have an $R_{ds(ON)}$ characteristic that increases strongly with temperature. From room temperature to maximum converter operating temperature (around 100□) the MOSFET $R_{ds(ON)}$ can increase by more than 50%. As the MOSFET temperature will increase proportionally to the current carried, this also provides a natural type of feedback mechanism that helps to further improve the passive current sharing of the ZIV converter when one phase is carrying a larger current. It should also be noted that this passive, droop current sharing technique, is also utilized by other 48V to 12V unregulated converters, including the cascaded resonant converter. As shown by the experimental results of these other converters, as well as previously and current experimental results for the ZIV converter, with a symmetrical layout it is possible to achieve excellent performance with only passive droop current sharing in these unregulated converters.

V. Experimental Results

Table 1 Experimental Prototype Components

Input Voltage	40V-60V
C_{in}	1x4.7uF 100V 1206
M1-M4	Infineon BSZ025N04LS (40V, 2.5mΩ)
C_{f1}	5x10uF 50V 1206 (top) 5x10uF 35V 0805 (bottom)
M5-M8 and Q5-Q8	Infineon BSZ017NE2LS5I (25V, 1.7mΩ)
C_{f2} and C_{f3}	3x47uF 25V 1210 (top) 4x10uF 35V 0805 (bottom)
C_{out}	3x47uF 25V 1210
L_1 and L_2	Coilcraft XEL4030-201 (200nH, 22A)
Switching Frequency	60kHz (120kHz M1-M4)

A. Component Selection

The components utilized for the experimental prototype are shown in Table 1. One phase of the experimental prototype is shown in Figures 11 and 12, showing the top and bottom sides of the converter. A single phase of the converter measures 1"x0.75"0.226", as measured by the smallest "box" that could completely contain the converter.

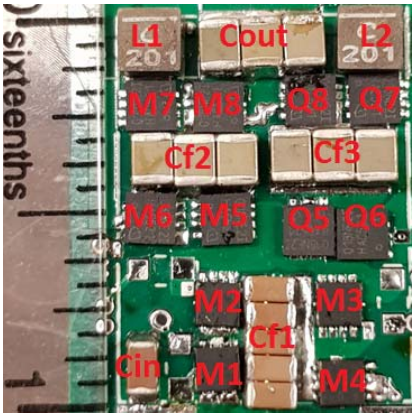

Figure 11 Top View For One Phase of Experimental Prototype (1"x0.75"x0.226")

On the top side of the experimental prototype the tallest component is the inductor, with a height of 0.126". Therefore, in order to optimize the performance of the converter, taller capacitors can be utilized on this side of the board to provide a larger capacitor value and lower ESR. On the bottom side of the board, the tallest component is the drivers with a height of 0.04" inches. Therefore, on the bottom side of the board 0805 size capacitors with a height of 0.04" are utilized in order to

minimize the overall height of the converter and achieve a much higher power density.

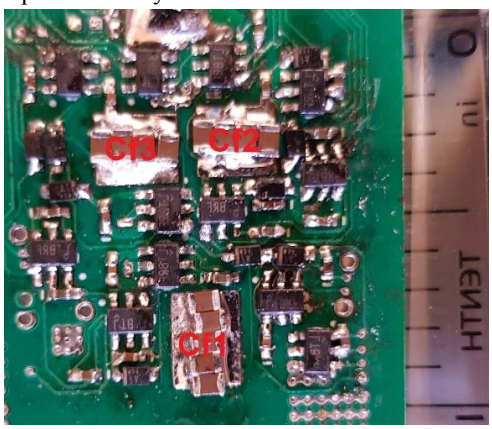

Figure 12 Bottom View for One Phase of Experimental Prototype (1"x0.75"x0.226")

The MOSFETs selected have a footprint of 3mm x 3mm. Larger MOSFET packages can offer improved performance, in particular by providing lower $R_{ds(ON)}$ for the same voltage rating. Additionally, the capacitors could be reduced in overall size by placing fewer of them in parallel. This would not negatively impact the operation of the converter significantly, as the ZIV converter does not rely on any resonant operation. However, this would increase the ESR of the capacitor banks, which would reduce the overall efficiency of the converter. Therefore, there is a very large degree of flexibility for designers to exchange power density for efficiency, and vice-versa. This flexibility cannot always be matched by designs that rely on specifically tuned resonant components.

As compared with a single phase 12-Switch ZIV converter [1], designed for similar output power level, the Two-Phase converter achieves more than double the power density. This is achieved through the significant reduction in input capacitor size, from 15x4.7uF capacitors to only 1x4.7uF, and the reduction in current stress of each individual component allowing for the use of smaller MOSFET package size (3mm by 3mm vs 6mm by 5mm) and smaller flying capacitors.
While a Two-Phase prototype is demonstrated in this work, it is also possible to further extend this to higher numbers of phases to achieve higher output current levels. It is optimal, however, to utilize an even number of phases. This is because each 12-Switch ZIV converter operates with 50% duty cycle on M1. By utilizing an even number of phases this allows for nearly perfect interleaving operation on the input capacitor, significantly reducing the RMS current through the input capacitor. As the input capacitor is the highest voltage stress component of the ZIV converter, it is often the largest component in single (or odd numbered) phase ZIV converter designs such as [20].

B. Converter Operation

Figure 13 shows the output voltage of 12V (CH1), as well as the C_{f1-1} ripple voltage (CH2), C_{f2-1} ripple voltage (CH3), and the voltage at the node (Node 2) before the output inductor (CH4) for the converter operating at 50A load with 48V input. Note that the inductor voltage is the difference between Node 2 and the output voltage, equal to the capacitor ripple voltage, allowing for the very small 200nH inductor to be used even with 60 kHz switching frequency. As the capacitors in a ZIV converter are never connected in parallel, the capacitor voltage ripple does not negatively impact the converter operation, unlike in a SC topology where the capacitor ripple must be minimized to reduce the charge redistribution loss, and additional inductors to achieve soft-charging are not required.

The measured output voltage characteristic for 48V input of the ZIV converter prototype is shown in Figure 14. Note that this linearly decreasing output voltage very closely matches the theoretical output voltage characteristic presented in Figure 9 for the ZIV converter.

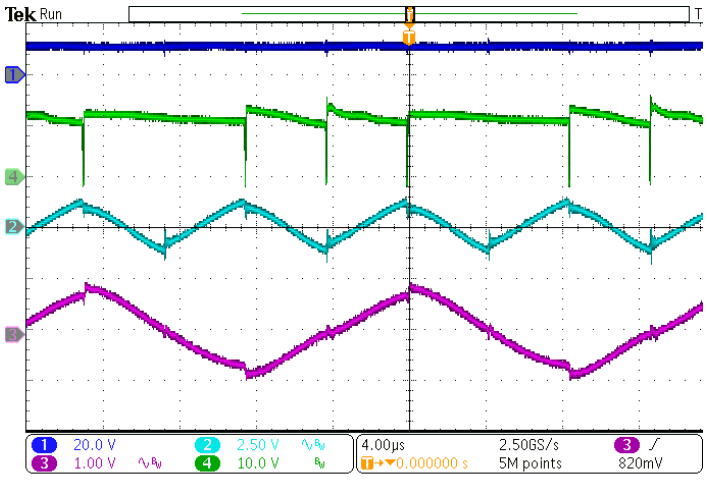

Figure 13 Experimental Prototype Waveforms for 48V Input 50A Load

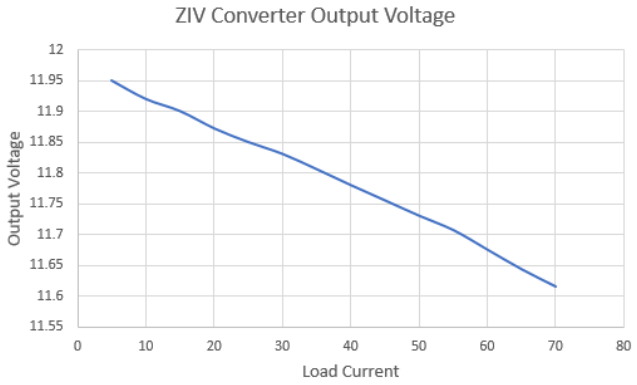

Figure 14 Experimental Prototype Measured Output Voltage Characteristic

C. Current Sharing

As discussed in Section IV-A the negative output voltage characteristic of the ZIV converter is the key enabler of passive current sharing. In order to validate the theoretical analysis, thermal images of the prototype are presented.

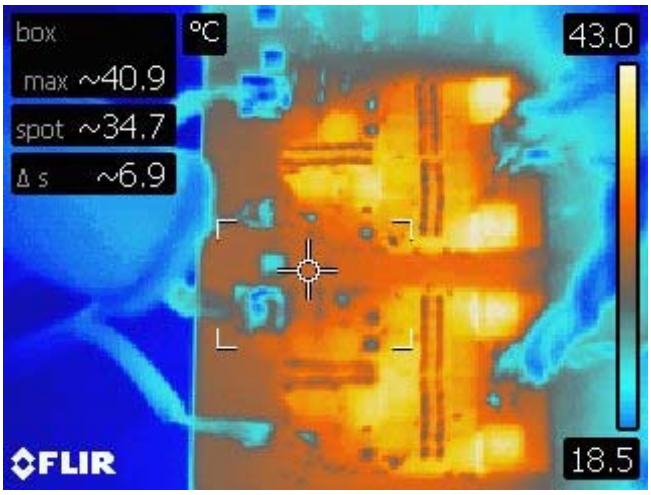

Figure 15 20A Load No Fan Cooling

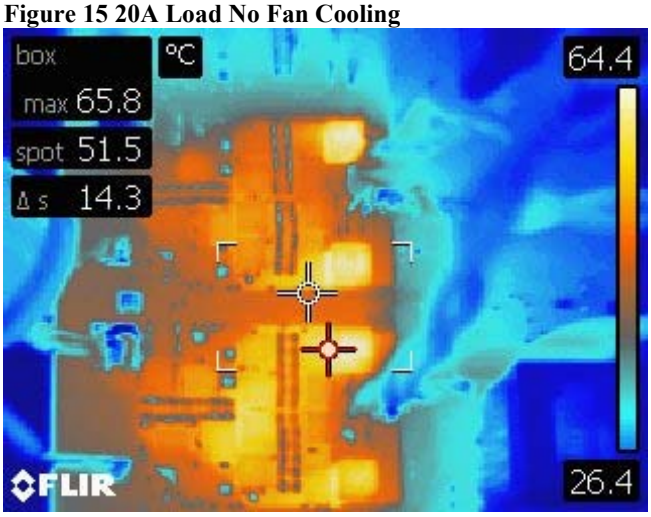

Figure 16 40A Load No Fan Cooling

Figures 15 and 16 show the thermal performance of the ZIV converter operating at 20A, and 40A output load respectively with no external fan cooling. The even thermal performance across both phases demonstrates that adequate current sharing performance is achieved passively due to the negative output voltage characteristic of the ZIV converter. Figure 17 shows the thermal performance of the ZIV converter operating at full 70A load for 48V input with a small USB desk fan used for cooling.

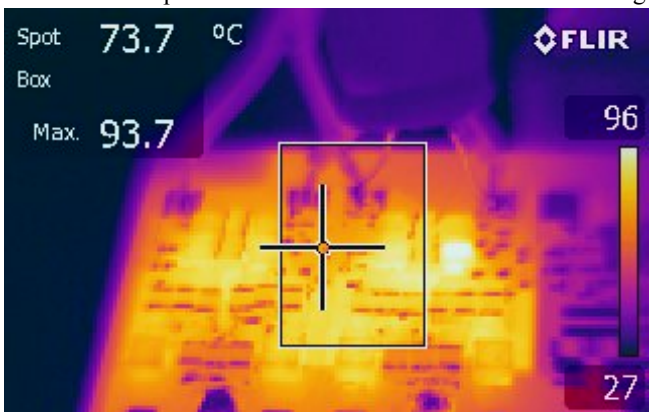

Figure 17 70A Full Load With Fan Cooling

D. Efficiency

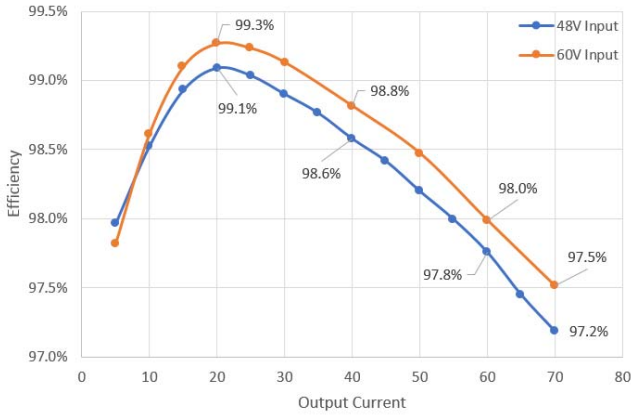

Figure 18 Measured Efficiency for Experimental Prototype Including Gate Drive Loss

For 48V to 12V input the maximum output current of the prototype is 70A, and the measured efficiency at this load condition (including gate drive loss) is 97.2%. The peak efficiency for the prototype is 99.1%. As compared with [18] which achieves 12V 60A efficiency of 97.2%, the ZIV converter prototype achieves a 12V 60A efficiency of 97.8%. Based on the full load current of 12V 70A output the converter power density is 2500W/in^3. This matches the highest power density yet demonstrated in literature by [18], which achieving higher overall efficiency. The efficiency measurements for the ZIV converter for both 48V and 60V input are presented in Figure 18. The measurements were taken using a Keithley 2700 digital multimeter, and Reidon RSN series (0.1% error) current shunts.

VI. Conclusions

The 12-Switch ZIV converter offers has several key characteristics that make it an ideal solution for 48V to 12V conversion in datacenter and server power supplies. According to [12] the key factors that have prevented wide-spread adoption of existing converter topologies are sensitivity to component variation or tolerances, inability to scale to differing power levels (particularly through paralleling), optimal utilization of semiconductor devices (50% duty cycle on all MOSFET pairs). The 12-Switch ZIV converter is able to meet all of these criteria. Without a resonant based design the ZIV converter guarantees excellent immunity to any variation in inductor or capacitor values, as any variation in these components will only change the ripple voltage or ripple current values slightly.

The ZIV converter is a conduction loss dominated converter. This is a particularly attractive feature as in a conduction loss dominated converter utilizing more phases, or components with lower resistance values (usually at the expense of size) give designers a great deal of flexibility to optimize a design for efficiency, or power density. As demonstrated by this work the

Table 2 Overview of 48V to 12V Converter Experimental Results

Converter Topology	Performance Metrics				
	Power Density	***Peak Efficiency***	***Full-Load Efficiency***	***# of Switches***	***Maximum Output Power***
Two-Phase 12-Switch ZIV (this work)	2500W/in^3	99.1%	97.2% (70A)	24	840W
Cascaded Resonant Converter (Two-Phase) [18]	2500W/in^3	99.1%	97.2% (60A)	16	720W
12-Switch ZIV [1]	990W/in^3	99.2%	97.8% (65A)	12	780W
Dickson SC [19]	400W/in^3	98.0%	96.9% (40A)	10	500W
Switched Tank [12]	500W/in^2	98.6%	97.4% (48A)	10	650W (13.5V output)

ZIV converter can achieve adequate current sharing passively. Therefore, multiple phases can always be used to achieve interleaving on the input capacitor, significantly improving performance, as well as allowing the converter to easily scale to differing power levels.

Table 2 presents a comparison between selected 48V to 12V bus converter topologies. The Two-Phase 12-Switch ZIV converter prototype presented achieves a power density of 2500W/in^3, equaling the highest yet demonstrated for 48V to 12V conversion by the cascaded resonant converter. Compared to the cascaded resonant converter, however, the ZIV converter achieves notably higher efficiency, with a peak efficiency of 99.1% a full load 12V 70A efficiency of 97.2%, and a 12V 60A efficiency of 97.8%. Comparatively the cascaded resonant converter achieves a 12V 60A efficiency of 97.2%. The ZIV converter thus achieves the best overall performance yet demonstrated for 48V to 12V conversion. While the ZIV converter utilizes a larger number of semiconductor components than many solutions, the ZIV converter substantially reduces the volume of passive components when compared with other 48V to 12V converters, allowing extremely high power density to be achieved. The 12-Switch ZIV converter also reduces the current stress of the individual semiconductor switches by using two output stages. Utilizing a larger number of semiconductor components can also be desirable as potentially packaging drivers and MOSFETs together could substantially reduce the overall size of the converter even further, especially compared with converter topologies that require larger capacitors and inductors that cannot achieve such size reductions.

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